Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1-9. (Cancelled).

10. (Previously presented) A multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate having a plurality of pixel regions arranged in arrays;

a second substrate positioned parallel to and directly above the first substrate;

a plurality of data lines positioned in each pixel region respectively;

a plurality of electrode patterns respectively positioned in each pixel region, each electrode pattern comprising a first electrode pattern, parallel to each data line, traversing a middle of each pixel region, and two second electrode patterns perpendicular to the first electrode pattern;

a plurality of pixel electrodes respectively positioned in each pixel region and above the electrode patterns, each pixel electrode comprising a plurality of slits which are parallel to the first electrode pattern;

a dielectric layer positioned between the electrode patterns and the pixel electrodes;

a liquid crystal layer positioned between the first substrate and the second substrate;

a common electrode layer positioned on a surface of the second substrate facing the first substrate; and

a plurality of protrusions positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with

each slit, wherein the protrusion in each pixel region is positioned above the first electrode pattern.

11. (Original) The multi-domain vertical alignment LCD panel of claim 10 further comprising a color filter layer positioned between the second substrate and the common electrode layer.

12. (Original) The multi-domain vertical alignment LCD panel of claim 10 further comprising a black matrix layer positioned on the surface of the second substrate facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

13. (Original) The multi-domain vertical alignment LCD panel of claim 10, wherein the electrode patterns are electrodes of storage capacitors.

14. (Original) The multi-domain vertical alignment LCD panel of claim 10, wherein the electrode patterns are electrically connected to one another.

15. (Previously presented) The multi-domain vertical alignment LCD panel of claim 10 further comprising a plurality of thin film transistor (TFTs) respectively positioned in each pixel region, wherein each data line is connected to a source of the TFT.

16. (Original) The multi-domain vertical alignment LCD panel of claim 15, wherein the electrode patterns serve as dummy circuits while the data lines are disconnected.

17. (Original) The multi-domain vertical alignment LCD panel of claim 10, wherein critical dimensions of the protrusions are less than those of the electrode patterns.

18. (Previously presented) The multi-domain vertical alignment LCD panel of claim 10, wherein each electrode pattern in the pixel region is arranged in I-shape.

19. (Withdrawn)A multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate having a plurality of pixel regions arranged in arrays;

a second substrate positioned parallel to and directly above the first substrate;

a plurality of data lines positioned in each pixel region;

a plurality of electrode patterns positioned in each pixel region, each electrode pattern comprising a first electrode pattern, perpendicular to each data line, traversing a middle of each pixel region, and two second electrode patterns perpendicular to the first electrode pattern;

a plurality of pixel electrodes positioned in each pixel region and above the electrode patterns, each pixel electrode comprising a plurality of slits which are parallel to the first electrode pattern;

a dielectric layer positioned between the electrode patterns and the pixel electrodes;

a liquid crystal layer positioned between the first substrate and the second substrate;

a common electrode layer positioned on a surface of the second substrate facing the first substrate; and

a plurality of protrusions positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit, wherein the protrusions located in the pixel region are positioned above the first electrode pattern respectively.

20. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 19 further comprising a color filter layer positioned between the second substrate and the common electrode layer.

21. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 19 further comprising a black matrix layer positioned on the surface of the second substrate facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

22. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 19, wherein the electrode patterns are electrodes of storage capacitors.

23. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 19 further comprising a plurality of thin film transistors (TFTs) positioned in each pixel region.

24. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 23, wherein each data line is electrically connected to a source of each thin film transistor.

25. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 24, wherein the electrode patterns serve as dummy circuits while the data lines are disconnected.

26. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 19, wherein critical dimensions of the protrusions are less than those of the electrode patterns.

27. (Withdrawn) The multi-domain vertical alignment LCD panel of claim 19, wherein each electrode pattern in the pixel region is arranged in H-shape.

28. (New) A multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate having a plurality of pixel regions arranged in arrays;

a second substrate positioned parallel to and directly above the first substrate;

a plurality of conductive lines positioned in each pixel region respectively;

a plurality of electrode patterns respectively positioned in each pixel region, each electrode pattern comprising a first electrode pattern, parallel to each conductive line, traversing a middle of each pixel region, and two second electrode patterns perpendicular to the first electrode pattern;

a plurality of pixel electrodes respectively positioned in each pixel region and above the electrode patterns, each pixel electrode comprising a plurality of slits which are parallel to the first electrode pattern;

a dielectric layer positioned between the electrode patterns and the pixel electrodes;

a liquid crystal layer positioned between the first substrate and the second substrate;

a common electrode layer positioned on a surface of the second substrate

facing the first substrate; and

a plurality of protrusions positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit, wherein the protrusion in each pixel region is positioned above the first electrode pattern.

29. (New) The multi-domain vertical alignment LCD panel of claim 28, wherein the conductive lines are data lines.

30. (New) The multi-domain vertical alignment LCD panel of claim 28, wherein the conductive lines are scan lines.

31. (New) The multi-domain vertical alignment LCD panel of claim 28 further comprising a color filter layer positioned between the second substrate and the common electrode layer.

32. (New) The multi-domain vertical alignment LCD panel of claim 28 further comprising a black matrix layer positioned on the surface of the second substrate facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

33. (New) The multi-domain vertical alignment LCD panel of claim 28, wherein the electrode patterns are electrodes of storage capacitors.

34. (New) The multi-domain vertical alignment LCD panel of claim 28 further comprising a plurality of thin film transistors (TFTs) positioned in each pixel region.

35. (New) The multi-domain vertical alignment LCD panel of claim 34, wherein each data line is electrically connected to a source of each thin film transistor.

36. (New) The multi-domain vertical alignment LCD panel of claim 35, wherein the electrode patterns serve as dummy circuits while the data lines are disconnected.

37. (New) The multi-domain vertical alignment LCD panel of claim 28, wherein critical dimensions of the protrusions are less than those of the electrode patterns.

38. (New) The multi-domain vertical alignment LCD panel of claim 28, wherein each electrode pattern in the pixel region is arranged in I-shape.

39. (New) The multi-domain vertical alignment LCD panel of claim 28, wherein each electrode pattern in the pixel region is arranged in H-shape.